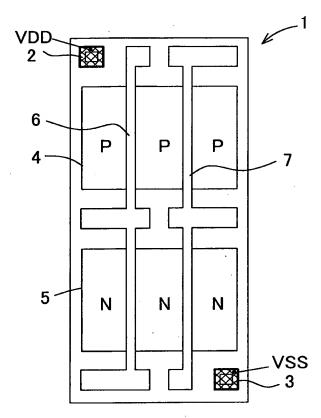
FIG. 1
FUNDAMENTAL CELL IN ACCORDANCE WITH THE PRESENT INVENTION



:LOWEST METAL WIRING LAYER(M1)

:UPPER METAL WIRING LAYER(M2)

£

Stendt auf? auf? auf? aff 12' ungel bienen. Ut Riebt Riebt Biene Band!

FIG. 2 FUNCTIONAL CIRCUIT BLOCK FORMED BY USING FUNDAMENTAL CELLS IN ACCORDANCE WITH THE PRESENT INVENTION

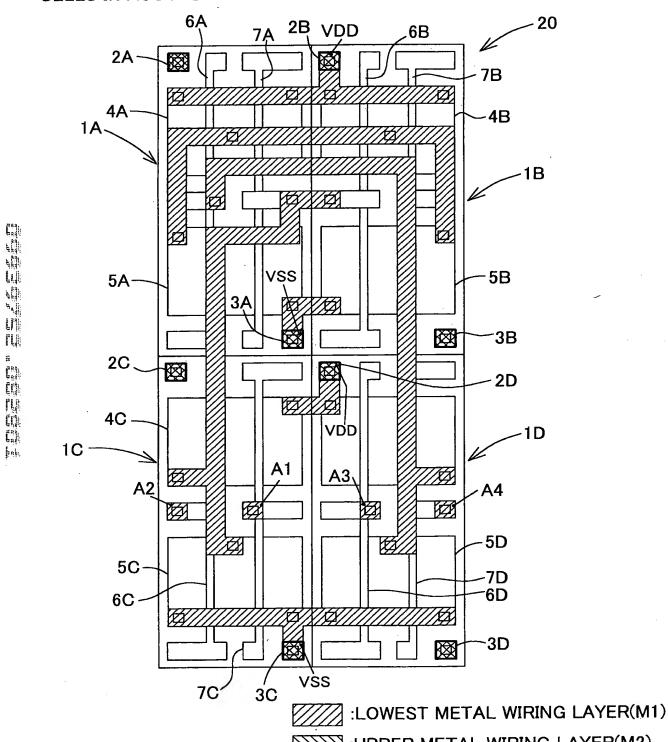
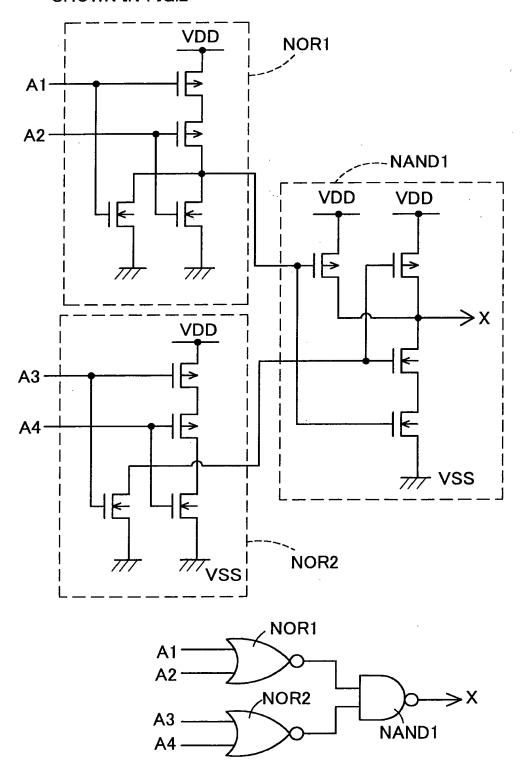


FIG. 3
CIRCUIT DIAGRAM OF THE FUNCTIONAL CIRCUIT BLOCK SHOWN IN FIG.2

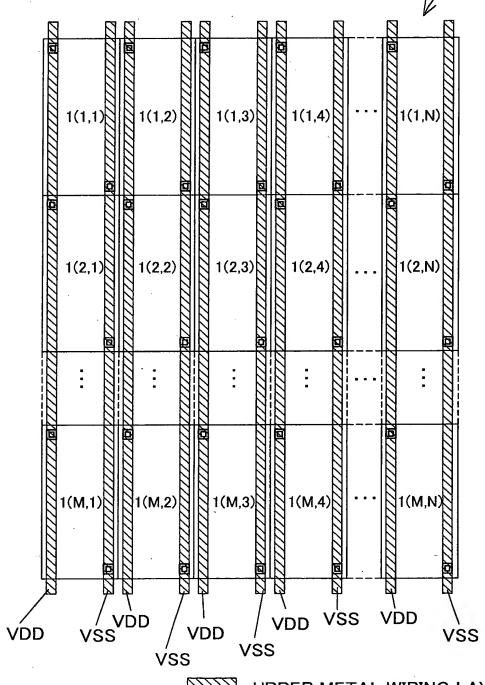


 FIRST PRACTICAL EMBODIMENT OF POWER RAILS WHEN THE FUNDAMENTAL CELLS IN ACCORDANCE WITH THE PRESENT INVENTION ARE ARRANGED IN A FORM OF MATRIX

				•			
$\square$			VOLTTI TO	10//////		10////m	₩ VDD
	1(1,1)	1(1,2)	1(1,3)	1(1,4)		1(1,N)	
<b>K</b> Z	TOTAL MARKET						☑ VSS
		70/////DI			7777	<i>101/////</i>	□ VDD
	1(2,1)	1(2,2)	1(2,3)	1(2,4)	•••	1(2,N)	
	7777777	(1/1/1/XX			7777	////// <b>///////////////////////////////</b>	☑ VSS
	÷	•	:	:	<b>.</b>	:	
$   \sqrt{} $	ADITION OF	101/1/10N	JOLL COLOR			7777778	ZZ VDD
	1(M,1)	1(M,2)	1(M,3)	1(M,4)		1(M,N)	⊠VSS
~~							

FIG. 5

SECOND PRACTICAL EMBODIMENT OF POWER RAILS WHEN THE FUNDAMENTAL CELLS IN ACCORDANCE WITH THE PRESENT INVENTION ARE ARRANGED IN A FORM OF MATRIX  $_{\sim32}$ 



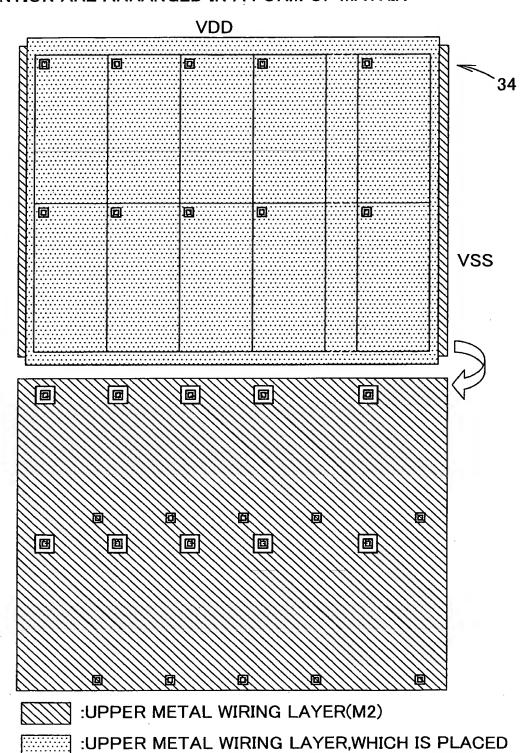
The state of the s

THIRD PRACTICAL EMBODIMENT OF POWER RAILS WHEN THE FUNDAMENTAL CELLS IN ACCORDANCE WITH THE PRESENT INVENTION ARE ARRANGED IN A FORM OF MATRIX

VDD VSS VDD VSS VDD vss

FIG. 7

FOURTH PRACTICAL EMBODIMENT OF POWER RAILS WHEN THE FUNDAMENTAL CELLS IN ACCORDANCE WITH THE PRESENT INVENTION ARE ARRANGED IN A FORM OF MATRIX



UPWARDLY OVER THE UPPER METAL WIRING

LAYER M2 (M3)

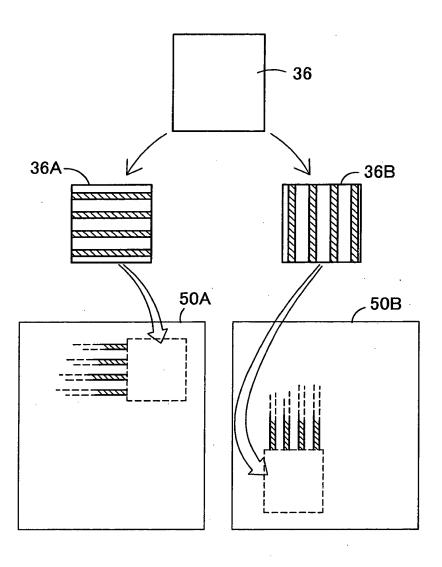
FIG. 8

FIFTH PRACTICAL EMBODIMENT OF POWER RAILS WHEN THE FUNDAMENTAL CELLS IN ACCORDANCE WITH THE PRESENT INVENTION ARE ARRANGED IN A FORM OF MATRIX

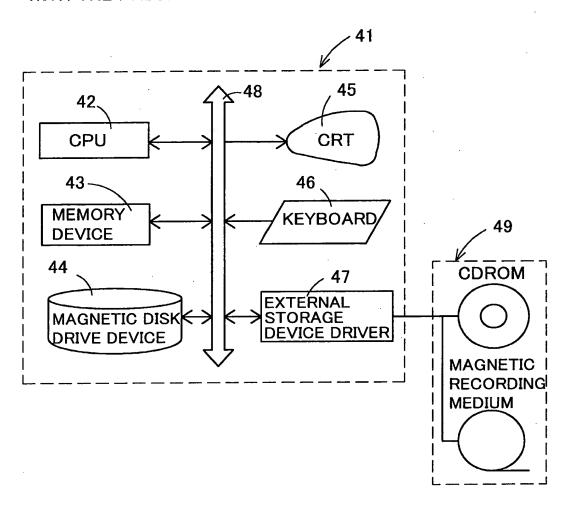
				<b>/</b> 35			
						V	
<u> </u>		(1) (1) (a)	10(/////	TOX (1)	777		₩ VDD
	<u> </u>		(I <del>-</del> K \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	131111111111111111111111111111111111111			L VDD
	1(1,1)	1(1,2)	1(1,3)	1(1,4)		1(1,N)	
		·		-VSS1			
$\overline{Z}$				7777770	777		ZZ VSS
$\square$	<b>W</b>	<b>IO</b>		<b>D</b>		10/////01	□ VDD
		L^	Marie Land	VDD1	·		
	1(2,1)	1(2,2)	1(2,3)	1(2,4)		1(2,N)	
$\overline{Z}$		////// <b>//</b>			777	77777778	⊠ VSS
	:	÷	.•	•		:	
$\square$	<b>10</b> /////	(A)			1111	1/////XX	⊠ ∧DD
	1(M,1)	1(M,2)	1(M,3)	1(M,4)	•••	1( <b>M</b> ,N)	
			////// <b>//</b>	777777 <b>7</b>	7777	777777 <b>7</b> 0	zsv <sub>zz</sub>

## FIG. 9

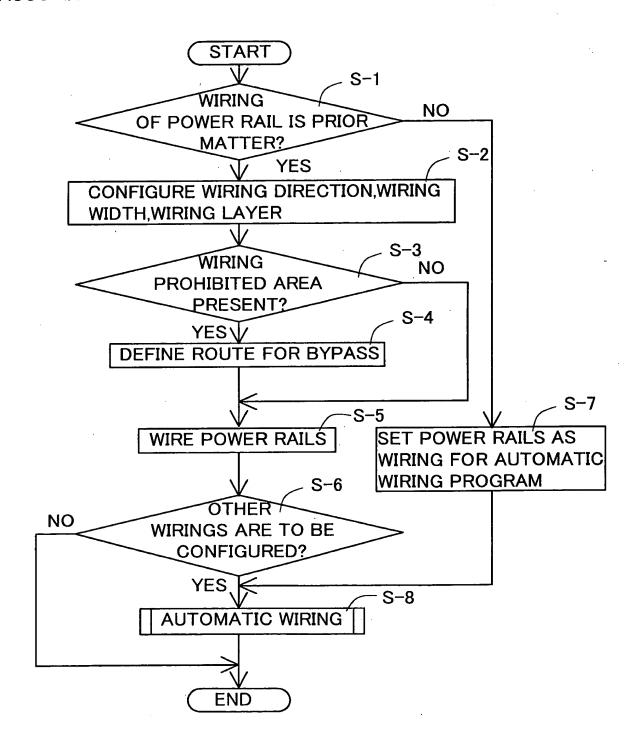
SIXTH PRACTICAL EMBODIMENT OF POWER RAILS WHEN THE FUNCTIONAL CIRCUIT BLOCKS IN ACCORDANCE WITH THE PRESENT INVENTION ARE ARRANGED TO FORM A SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE



BLOCK DIAGRAM OF A WIRING APPARATUS IN ACCORDANCE WITH THE PRESENT INVENTION

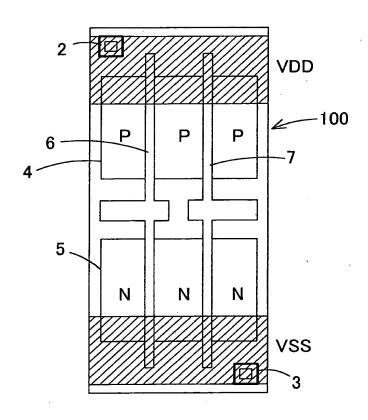


# FIG. 11 A FLOW CHART OF A WIRING METHOD FOR WIRING IN A FUNCTIONAL CIRCUIT BLOCK USING THE FUNCTIONAL CIRCUIT BLOCKS IN ACCORDANCE WITH THE PRESENT INVENTION



## FIG. 12 PRIOR ART

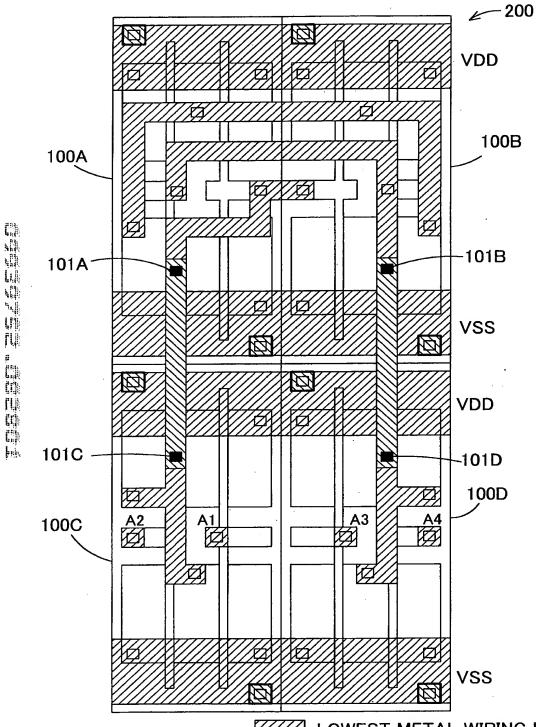
### FUNDAMENTAL CELL IN ACCORDANCE WITH THE RELATED ART



:LOWEST METAL WIRING LAYER(M1)

FIG. 13 PRIOR ART

FUNCTIONAL CIRCUIT BLOCK FORMED BY USING THE FUNDAMENTAL CELLS OF THE RELATED ART



:LOWEST METAL WIRING LAYER(M1)
:UPPER METAL WIRING LAYER(M2)





## FIG. 14 PRIOR ART

POWER RAIL EMBODIMENT WHEN FORMING THE FUNDAMENTAL CELLS OF THE RELATED ART IN A FORM OF MATRIX

					/ 30	00
						VDD
100(1,1)	100(1,2)	100(1,3)	100(1,4)		100(1,N)	
						<del>7.</del> 7
						vss
						VDD
100(2,1)	100(2,2)	100(2,3)	100(2,4)		100(2,N)	
						vss
:	-	•	:		•. •	
			1			
						VDD
100(M,1)	100(M,2)	100(M,3)	100(M,4)		100(M,N)	
						vss
				L	<u> </u>	

:LOWEST METAL WIRING LAYER(M1)